

**AMENDMENTS TO THE CLAIMS**

1. (Previously Presented) A processor, comprising:
  - a cryptocoprocessor having:
    - an arithmetic unit for processing operands;
    - a register memory for storing operands; and a register memory configuration unit designed to configure the register memory such that memory space in the register memory is assigned to operands and that memory space in the register memory that is not assigned to operands is made available for data other than the operands;
  - a volatile working memory comprising:
    - an external working memory, the external working memory being physically disposed outside the cryptocoprocessor; and
    - the register memory space not assigned to operands, the register memory space being physically disposed within the cryptocoprocessor,
  - wherein at least a part of the register memory space not assigned to operands is mapped into the working memory, and
  - an address unit operable to address the register memory space not assigned to operands and being physically disposed within the cryptocoprocessor in the same way as the external working memory being physically disposed outside the cryptocoprocessor.
2. (Original) The processor according to claim 1, wherein the arithmetic unit, the register memory and a control unit for controlling the arithmetic unit and the register memory for loading operands from the register memory into the arithmetic unit and for carrying out an operation with the operands are designed as integrated circuit on a single chip.
3. (Original) The processor according to claim 1, wherein the operands are long number operands comprising a length of more than 150 bits.

4. (Cancelled)

5. (Currently Amended) The processor according to claim 1, wherein the arithmetic unit is adapted designed to perform at least two algorithms, wherein one algorithm needs a maximum amount of register memory space due to its length and/or number of its used operands, while another algorithm needs a smaller amount of register memory space for its operands,

wherein the register memory is dimensioned such that the register memory space is at least equal to the maximum amount of register memory space needed by an algorithm for its operation.

6. (Currently Amended) The processor according to claim 1, which is adapted designed to carry out a cryptographic algorithm.

7. (Original) The processor according to claim 1, wherein the arithmetic unit and the register memory are connected via an internal bus,

wherein an external element is connected to the arithmetic unit via an external bus, and

wherein the length of the external bus is greater than the length of the internal bus.

8. (Original) The processor according to claim 1, wherein the register memory configuration unit is disposed to configure registers of different number and length in the register memory as needed.

9. (Withdrawn) A computer system, comprising:  
a host CPU;  
a peripheral device connected to the host CPU via an external bus, the peripheral device comprising an internal memory; and

a memory configuration unit, the memory configuration unit being designed to make space from the internal memory available for the peripheral device as needed, and to make space from the internal memory not being made available to the peripheral device available for other data by access via an external bus;

a volatile working memory comprising:

an external working memory being physically disposed outside the peripheral device; and

the internal memory space being available for other data by access via an external bus, which is physically disposed within the peripheral device,

wherein at least a part of the internal memory space being available for other data by access via an external bus is mapped into the working memory; and

an address unit operable to address the internal memory space being available for other data by access via an external bus, and being physically disposed within the peripheral device in the same way as the external working memory being physically disposed outside the peripheral device.

10. (Canceled)

11. (Withdrawn) The computer system according to claim 9, wherein the memory configuration unit is part of the peripheral device.

12. (Withdrawn) The computer system according to claim 9, wherein the memory configuration unit is disposed to check whether the peripheral device is active and in the case when the peripheral device is not active, to make the whole internal memory of the peripheral device available for the computer system as working memory.

13. (Withdrawn) The computer system according to claim 9, wherein the peripheral device is a cryptocoprocessor.

14. (Withdrawn) The computer system according to claim 9, designed as chip card IC or security IC.

15.-16. (Canceled)